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Electrical and optical properties of thin film (n)CdSe/(p)CdTe heterojunction and its performance as a photovoltaic converter

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Thin film (n)CdSe/(p)CdTe heterojunctions were fabricated by depositing p-type CdTe thin films on n-type CdSe thin films using the thermal evaporation technique, and their electrical and optical properties at room temperature as well as elevated temperatures have been investigated by current-voltage measurements. The different junction parameters such as diode ideality factors, barrier heights, Richardson constant, short-circuit currents, open circuit voltage, etc. were determined from I-V characteristics and found changing on vacuum annealing. The ideality factors (> 2 in dark at 303K) were found to decrease with increase in temperature. At room temperature (303K), the barrier height was found to be 0.7eV in dark and showed no temperature dependence in the range from 303K to 333K. The photovoltaic performance of the junction was found to improve on vacuum annealing. The structure with concentrations N_a=2.43x10^{16}/cm^3 for CdTe and N_d= 9.03×10^{15}/cm^3 for CdSe showed a photovoltaic effect with fill factor 0.46, open-circuit voltage 135 mV, short-circuit current 2.06×10^{-4}A/cm^2 for an annealed sample and corresponding quantities 0.37, 148 mV, 1.9×10^{-4}A/cm^2 for an untreated sample. The fill factor was found to decrease with increase in temperature. The junctions exhibited spectral response within 550-900 nm giving a peak at wave length 762 nm. Proper doping and annealing lead to reduction of series resistance for achieving an ideal solar cell.

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Keywords: Heterojunction, Annealing, Photovoltaic effect, Spectral response

1. Introduction

In recent years, heterojunctions belonging to the II-IV family have received much attention because of their potential optoelectronic applications over a wide range of wavelengths [1,2]. CdSe and CdTe are two highly photosensitive semiconductors having direct band gap and with large absorption coefficient in the visible region of solar spectrum [3]. These properties have lead to the investigations of CdSe and CdTe based heterojunctions and Schottky barrier junctions for photovoltaic applications [1, 2, 4]. CdTe is an amphotaric compound whereas CdSe can be made n-type. Moreover lattice mismatch between them is also small. There are literatures on (n)CdSe/(p)CdTe junction based on single-crystals [2]. Reports on CdSe film junctions with CIGS [5] and CdTe are also available. Although many investigations on the formation of Schottky barrier with single crystal bulk CdSe and CdTe using different metals and their heterojunctions have been done so far [2, 6], it is felt that a little attention is given to heterojunctions of polycrystalline CdSe and CdTe thin films. These films are mostly in undoped states and their studies are limited to current transport phenomena. Several techniques such as thermal evaporation [7, 8, 9], spray pyrolysis [10], CBD [11, 12], sputtering etc [13] have been used up to now for the fabrication of these junctions. In this paper we have reported several aspects of these junctions prepared by thermal evaporation with special reference to heat treatment of the junctions. The films were doped and vacuum annealed after deposition. The performance of these junctions as photovoltaic converter is also discussed.

2. Experimental

High purity (99.996%) CdSe and CdTe powder (Sigma Aldric, USA) were used for the preparation of the films and junctions by thermal evaporation. The junctions were fabricated in the same vacuum chamber under the pressure better than10^{-5} torr pressure. Chemically cleaned glass substrates were used in the chamber separately for the films and the junctions using suitable musk and source shutter. Ag and Sb metal were used for doping of CdSe and CdTe respectively. The sequential process of junction fabrication is as follows. At first, Al strips each of 0.1cm width as the base electrodes were vacuum deposited on the glass substrates. Above these, Ag-doped CdSe films of area 1.5×1.5 cm^2 were thermally deposited by co-evaporation of CdSe powder from electrically heated molybdenum boat and Ag metal (99.99%) from tungsten spiral filament. The substrate temperature for CdSe film deposition was kept constant at about 473K. The CdSe

film was then annealed at 523K in high vacuum for 30 minutes in order to ensure crystallization of the film. In the second step, strips of Sb doped CdTe films (as shown in fig. 1) were deposited onto CdSe films at substrate temperature 333K making crosses with Al strips. The junctions were then annealed in vacuum at 373K for 1 hour to ensure their stable electrical measurement. Finally Au strips each of 0.1cm width of rectangular size were vacuum evaporated perpendicularly to the Al strips using suitable mask. Thus on a single substrate nine Al-(n)CdSe/(p)CdTe-Au structures were obtained. One set of unannealed junctions were also prepared for study and to see the difference of performance between the annealed and unannealed junctions. A schematic diagram of a device structure having 9 Al-(n)CdSe/(p)CdTe-Au junctions of area 0.01 cm^2 each is shown in Fig.1.

For measurement of conductivity type, thickness and other studies, separate films were deposited at the time of respective semiconducting film deposition by placing additional substrates. Al electrodes were vacuum deposited on CdSe films for conductivity measurements. The thicknesses of the films were measured by multiple interference technique [14]. The conductivity type and carrier concentration of the films were determined by Hall effect measurement of the films and capacitance-voltage study [15] of the Schottky barriers. For films of lower doping concentration, the hot probe method [16] was also used to confirm the conductivity type of the film.

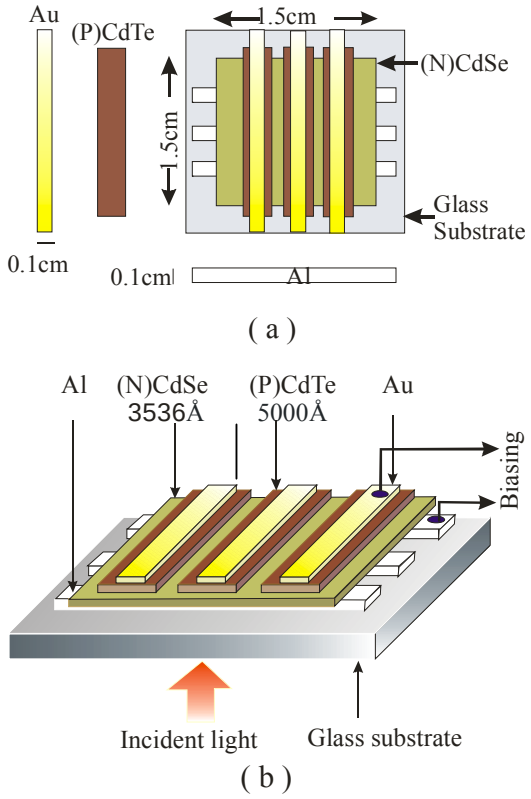

Fig. 1. Al-(n)CdSe/(p)CdTe-Au structure: (a) top view and (b) lateral view (not to scale).

To avoid effect of humidity, all electrical and photovoltaic measurements were studied in vacuum of 10^{-2} Torr by mounting the sample inside a specially assembled vacuum chamber. The details of this experimental arrangement have been discussed elsewhere [17]. A Kiethley system electrometer (model 6514) has been used to measure the current in dark and under illumination. The current (I)-voltage(V) characteristics of the junctions was recorded at room temperature as well as at elevated temperatures using heating arrangement with a temperature controller in the vacuum chamber. For studying the current–voltage characteristics under illumination, the samples in the chamber were illuminated through glass window using a white light from a tungsten-halogen lamp.

The spectral response of the junction was observed in the range of wavwlength from 400nm to 900nm with a monochromator (model 77200, Oriel instruments,U.S.A.).

3. Results and discussion

3.1 Current–voltage characteristics

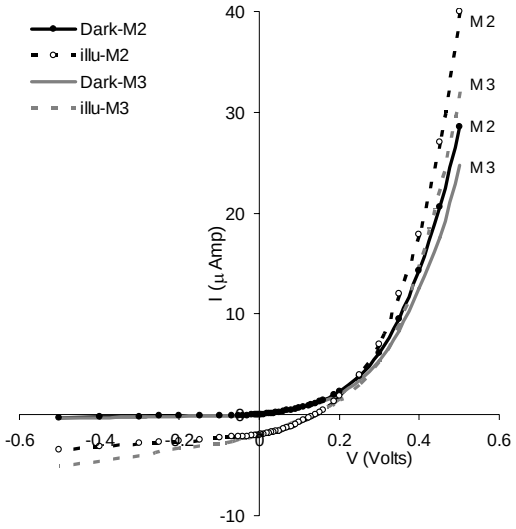

Fig.2. I-V plots of two typical samples under forward bias in dark (solid line) and illumination (dotted line).

The electrical contact between Al (work function W_F = 4.1eV) and (n)CdSe (electron affinity χ = 4.56 eV) [2] and between Au (W_F = 4.1eV) and (p)CdTe (electron affinity χ = 4.28 eV) [18] are ohmic as tested in these films separately. Figure 2 shows the *I-V* characteristics of two typical Al-(n)CdSe/(p)CdTe-Au junctions in dark and under illumination, at room temperature (303K). The rectifying behaviour of forward current of the fabricated junctions indicated the formation of a barrier.

The junction was illuminated with a light of 5000 lux to see the affect on the I-V characteristics. Annealed junctions are found to show higher forward current (Fig.3). The current density J of a diode of ideality factor n, for

biasing voltage V_a and at temperature T is given by the relation [19],

$$J = \frac{qA^*TV_{bi}}{k}\exp\left(-\frac{qV_{bi}}{kT}\right)\left[\exp\left(\frac{qV_a}{nkT}\right)-1\right] \quad (1)$$

where A^* is the Richardson constant and V_{bi} is the built in potential. This can be written in terms of saturation current density J_0 as

$$J = J_0\left[\exp\left(\frac{qV_a}{nkT}\right)-1\right] \quad (2)$$

where

$$J_0 = \frac{qA^*TV_{bi}}{k}\exp\left(-\frac{qV_{bi}}{kT}\right) \quad (3)$$

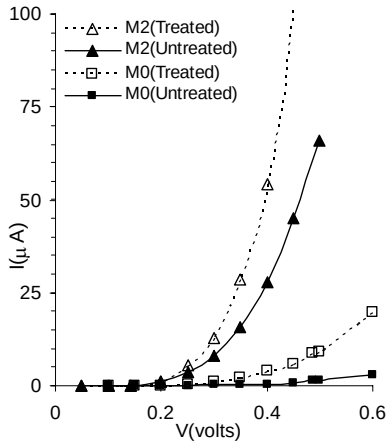

Fig. 3. I-V plots at room temperature in dark (solid line) and after heat treatment (doted line) for Al-(n)CdSe/(p)CdTe-Au junctions for different doping concentrations [$N_a = 1.03\times10^{15}$ cm^{-3} and $N_d = 7.32\times10^{14}$ cm^{-3} (for sample M0); $N_a = 2.43\times10^{16}$ cm^{-3} and $N_d = 9.03\times10^{15}$ cm^{-3} (for sample M2)].

The ideality factor(n) and the saturation current density (J_0) of different junctions as prepared (U) and after heat treatment (T) were calculated from the slopes and intercepts of the respective ln J vs V plots of them and are tabulated in Table2. The diode ideality factor for the structure was found greater than unity and has been lowered on heat treatment of the structures. However, the structure with semiconductor of higher doping concentration showed improvement of diode quality with reduced diode ideality factor.

At forward voltages above 0.2 volts, the ln$I$-V plots of the junctions have been observed to deviate from linearity (Fig.4). It is due to the effect of series resistance R_s associated with the neutral region of the semiconductor [20]. At large forward current (I) through the diode, the voltage drop across the series resistance causes the actual voltage drop across the barrier to be less than the voltage applied to the terminals of the junction. Hence, the current is proportional to [exp{$q(V$-$IR_s)/kT$}-1], instead of obeying the ideal condition. The horizontal displacement between the actual ln$I$-V curve and extrapolation of the linear region gives the voltage drop ΔV=IR_s across the neutral region.

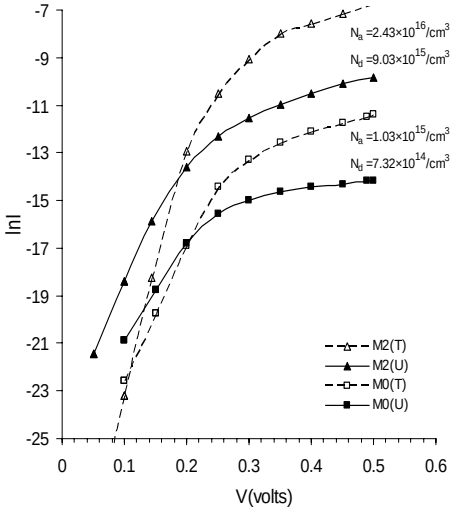

Fig.4. lnI versus V plots to determine the deviation ΔV from linearity at different currents.

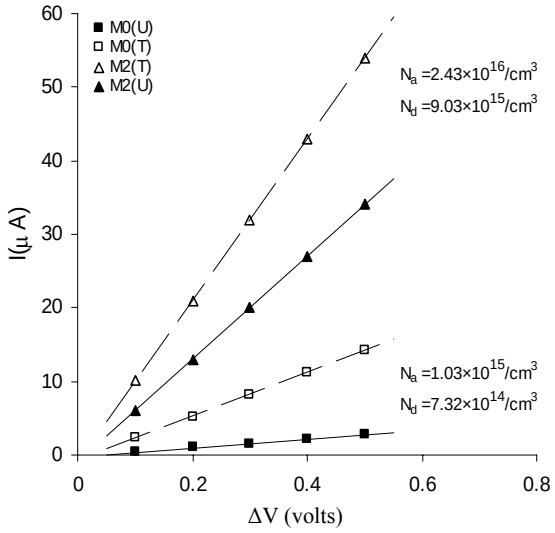

Fig. 5. I versus ΔV plots to determine series resistance of the junctions

The series resistance of these typical junctions calculated from the I vs ΔV plots (Fig. 5) are given in Table 1. The series resistance so obtained was found to be in the order of KΩ. The large value of series resistance is due to various types of defects which were crept into the films during preparation and also due to low doping concentration. The series resistance of the junctions of

higher doping concentration was found less. Introduction of any insulating layer between electrode and semiconductor also contributes to the series resistance. Heat treatment of the devices reduces the defects of the film and also makes more intimate contact between the electrodes and semiconductor by thermally removing the insulating layer. Therefore series resistance of the devices is found to be lowered on heat treatment.

The temperature dependence of *J-V* characteristics of the junction has been studied within the temperature range 300 K to 333 K. It has been observed that beyond room temperature, thermal generation of extra carriers causes a gradual increase of forward current. Figure 6 shows ln*J* vs *V* plots of the linear portion for a typical Al-(n)CdSe/(p)CdTe-Au junction at different temperatures from which the J_0 values at different temperatures were calculated. At all temperatures, the ideality factors *n* were found to be of nearly same value and the saturation current density J_0 was found to increase with temperature. When $\ln(J_0/T)$ vs T^{-1} is plotted (Fig. 7), straight lines are found for a typical as prepared junction in dark (solid line) and after heat treatment (dotted line).

The value of the effective Richardson constant A^* was calculated from the intercept on the vertical axis of the plots and was found to be around 46 $A.cm^{-2}.K^{-2}$ for as prepared junction and 115 $A.cm^{-2}.K^{-2}$ for annealed junction. This value was used to find the barrier height of the junction. The barrier height obtained in this junction was 0.63 for untreated and 0.7 eV for heat treated junction (Table 1) and found unaffected by the change of temperature.

The doping concentration is one of the major contributions on junction characteristics. In this case, the built-in potential (V_{bi}) plays an important role in the conduction mechanism. The usual relation for these two parameters can be written as

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{4}$$

Here, n_i is the intrinsic carrier concentration, N_a is the acceptor concentration and N_d is the donor concentration. Thus, it is clear from equations (3) and (4) that the value of saturation current density J_0 increases with an increase of V_{bi} due to an increase of doping concentrations N_a and N_d.

It is seen that there are no significant change of barrier height with doping concentrations. The lower value of barrier height may be due to the presence of interfacial layer. In polycrystalline semiconductor thin films, the constituent atoms at the grain boundary are disordered and hence there are large numbers of defects due to incomplete atomic bonding (dangling bond). This may result the existence of surface states [21].

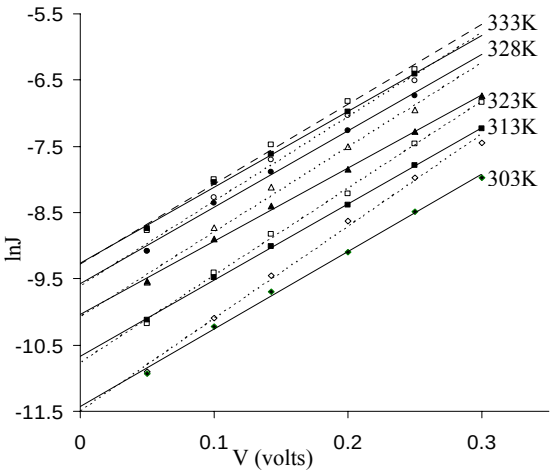

Fig.6. lnJ versus V plots in dark (solid line) and after heat treatment (doted line) for a typical Al-(n)CdSe/(p)CdTe-Au junction (M2) for doping concentration ($N_a = 2.43\times10^{16}$ cm^{-3} and $N_d = 9.03\times10^{15}$ cm^{-3}) at different temperatures.

In our case, the barrier heights have been found to be less dependent on the electron affinities of the semiconductors. This may be due to the effect of surface states of the semiconductor [22].

The presence of interfacial layer, image force lowering and carrier recombination due to surface states or defect levels are some of the main reasons for ideality factor to be greater than unity.

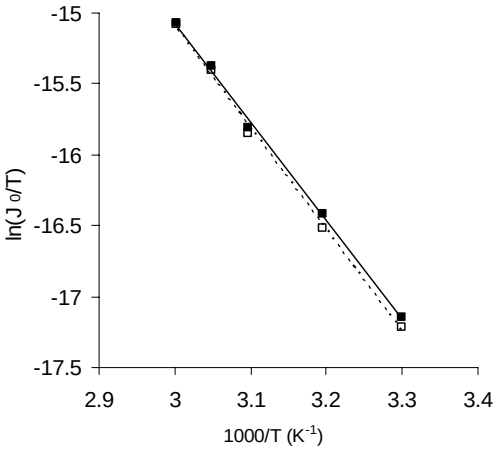

Fig. 7. $\ln(J_0/T)$ versus T^{-1} plots in dark (solid line) and after heat treatment (doted line) for a typical Al-(n)CdSe/(p)CdTe-Au junction (M2)

Heat treatment of the devices lowers the diode ideality factor and increases the barrier heights.This improvement is thought to be mainly due to formation of more intimate contact at the junction on heat treatment, avoiding any

surface irregularities, which can cause deviation from diode rectifying behavior. Heat treatment also removes interfacial layer and reduces the interface state densities.

Table 1. Values of series resistance for two typical Al-(n)CdSe/(p)CdTe-Au junctions at room temperature.

Junction number	Doping concentration (cm^{-3})		Series resistance (KΩ)	
	N_a	N_d	*U*	*T*
M0	1.03×10^{15}	7.32×10^{14}	130	35
M2	2.43×10^{16}	9.03×10^{15}	15	9

Table 2. Variation of junction parameters of a typical as-prepared (U) and heat treated (T) Al-(n)CdTe/CdSe-Au heterojunction (area=0.01 cm^{-2}) in dark.

Sample M2	Temp. (K)	Saturation current density J_0 (10^{-5}A.cm^{-2})		Ideality factor *n*		Built in potential V_{bi} (eV)		Richardson constant A^* (A.cm^{-2}.K^{-2})	
		U	*T*	*U*	*T*	*U*	*T*	*U*	*T*
$N_a=2.43\times10^{16}$ cm^{-3} $N_d=9.03\times10^{15}$ cm^{-3}	303	1.08	1.01	3.33	2.74	0.63	0.70	46	93
	313	2.33	2.09	3.21	2.81				
	323	4.39	4.21	3.25	2.80				
	328	6.91	6.70	3.08	2.77				
	333	9.48	9.37	2.97	2.88				

3.2 Photovoltaic effect

3.2.1. J-V characteristics under illumination

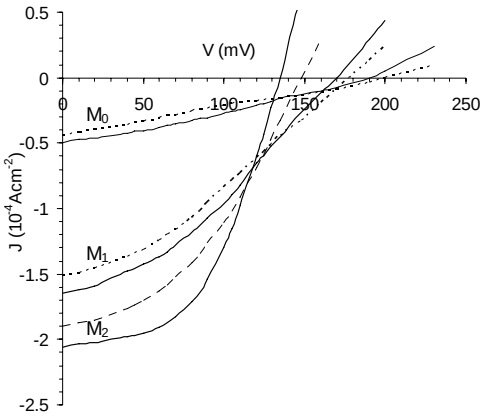

Fig. 8. Photovoltaic plots of as prepared (dotted curve) and heat treated (solid curve) Al-(n)CdSe/(p)CdTe-Au junctions of different doping concentrations [$N_a=1.03\times10^{15}$ cm^{-3} & $N_d=7.32\times10^{14}$ cm^{-3} (M_0); $N_a=7.21\times10^{15}$ cm^{-3} & $N_d=2.11\times10^{15}$ cm^{-3} (M_1); $N_a=2.43\times10^{16}$ cm^{-3} & $N_d=9.03\times10^{15}$ cm^{-3} (M_2)] at room temperature.

The Al-(n)CdSe/(p)CdTe-Au junctions were studied under illumination for their photovoltaic performance. Figure 8 shows the photovoltaic effect of three typical junctions of different doping concentrations under illumination of 5500 lux. At lower doping concentrations, the nearly linear nature of the *J-V* curve under illumination implies the existence of very large series resistance in the junctions. The open-circuit voltage (V_{oc}), short-circuit current (I_{sc}) and fill factor of these junctions are tabulated in Table 3. The short circuit current was found to increase from 0.44×10^{-4}A/cm^2 to 1.90×10^{-4}A/cm^2 with the increase of doping concentrations of the junctions. These values were found to increase up to 0.50×10^{-4}A/cm^2 and 2.06×10^{-4}A/cm^2 after heat treatment. The fill factor of the junctions was increased from 0.28 to 0.37 with the increase of doping concentration and was further increased up to 0.46 after heat treatment.

The open-circuit voltage (V_{oc}) and short-circuit current (I_{sc}) are strongly dependent on the series resistance (R_s) as well as on diode ideality factor (n) as per the well known equations [23]

$$I_{SC} = I_0\left[\exp\left(\frac{q(V-IR_S)}{kT}\right)-1\right]-I \quad (5)$$

$$V_{OC} = \frac{nkT}{q}\ln\left(\frac{I_{SC}}{I_0}+1\right) \quad (6)$$

where, I is the total output current and I_0 is the diode saturation current. In our case the higher value of series resistance reduces the short circuit current and hence the open circuit voltage also. Very low photo voltages with low value of fill factors have been observed in these junctions due to higher value of diode ideality factors. In the polycrystalline films, the grain boundary potential may affect the series resistance and open-circuit voltage of solar cell [24]. Recombination of photo generated carriers takes place at grain boundary and hence the short-circuit

current is reduced [24, 25]. Besides the affect of high series resistance and grain boundary effect, there are various factors responsible for the poor photovoltaic performance, such as high defect density, presence of interfacial layer and low doping concentration. The increase of doping concentration of the semiconducting films improves the photovoltaic performance of the devices. Improvement of photovoltaic performance was also observed in heat treated devices. This is mainly due to lowering of series resistance and improvement of diode quality.

Table 3. Photovoltaic parameters of as-prepared (U) and heat treated (T) Al-(n)CdSe/(p)CdTe-Au heterojunctions of area=0.01cm^2

Junction number	Doping concentration (cm^{-3})		Short circuit current density J_{SC} (10^{-4}A/cm^2)		Open circuit voltage V_{OC} (mV)		Fill factor *ff*	
	N_a	N_d	*U*	*T*	*U*	*T*	*U*	*T*
M_0	1.03×10^{15}	7.32×10^{14}	0.44	0.50	202	190	0.28	0.29
M_1	7.21×10^{15}	2.11×10^{15}	1.51	1.64	176	170	0.30	0.35
M_2	2.43×10^{16}	9.03×10^{15}	1.90	2.06	148	135	0.37	0.46

3.2.2. Temperature dependence of cell parameters

The current-voltage characteristics at measurement temperatures from 303 K to 328 K are shown in Fig. 9. The relations between V_{OC}, J_{SC}, *ff* and maximum power output P_{max} and the measurement temperature as obtained from Fig. 7 are tabulated in Table 4. *V*oc, *ff* and P_{max} are found to decrease and J_{SC} to increase as temperature rises. Thus within temperature range 303 K to 328 K, the junction showed maximum performance at room temperature (303 K) which deceases as the temperature rises. At 303 K, the cell characteristics are V_{OC} =135 mV, J_{SC} = 2.06×10^{-4} A/cm^2, *ff* = 0.35, P_{max}= 9.66×10^{-3} mW/cm^2.

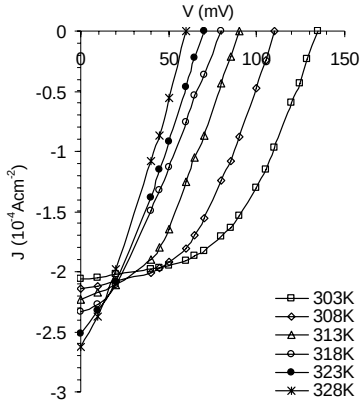

Fig. 9. Change in J-V characteristics under illumination with temperature.

Table 4. Temperature dependence of cell parameters.

Temperature(K)	V_{OC} (mV)	J_{SC} (10^{-4}Acm^{-2})	*ff*	P_{max} (10^{-3}mW/cm^2)
303	135	2.06	0.46	13.68
308	110	2.14	0.40	10.86
313	90	2.34	0.37	7.61
318	80	2.33	0.26	4.82
323	68	2.48	0.24	4.15
328	60	2.62	0.19	2.28

3.2.3. Spectral response

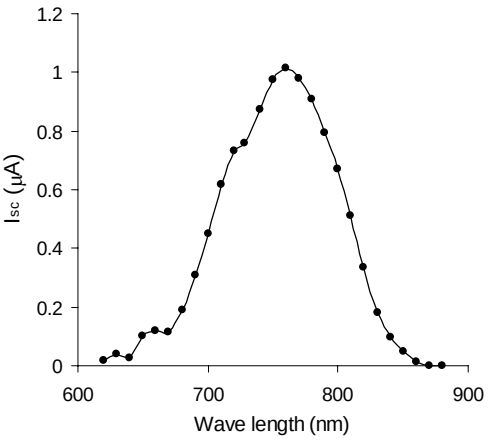

Fig.10. I_{SC} spectral response of CdSe/CdTe junction

The junction exhibited a spectral response in the range 600-900 nm. The maximum short circuit current was obtained corresponding to the wavelength about 762nm which is well within the visible region (Fig.10). The value of the band edge calculated from this peak was found to be 1.63eV which implies the absorption mostly within CdSe layer of the structure.

4. Conclusions

The results show the formation of rectifying barrier in thermally deposited Au-(n)CdSe/(p)CdTe-Al thin film structures. The diode is characterized by non-saturating and bias dependent reverse current and higher values of diode ideality factor. The junction exhibited low photovoltaic effect. Due to various types of defects and low doping concentration, the junctions have high series resistance. Presence of interfacial layer, surface states, various defects and high series resistance affect the *I-V* characteristics and photovoltaic effect. The performance of

the junction was improved after heat treatment. Proper doping, annealing and passivation of surface states are necessary to improve the diode quality and photovoltaic effect. The deposition of all the layers in one vacuum cycle might be advantageous. Further work is in progress in this direction.

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References

[1] F. Buch, A.L. Fahrenbruch, R. H. Bube, Appl. Phys. lett. **28**, 593 (1976).
[2] F. Buch, A.L. Fahrenbruch and R. H. Bube, J. Appl. Phys. **48**, 1596 (1977).
[3] M. B. Prince, J. Appl. Phys. **26**, 534(1955), J. J. Loferski, J. Appl. Phys. **27**, 777 (1956).
[4] C. F. Brucker, L. J. Brillson, Appl. Phys. Lett. **39**, 67 (1981).
[5] P. Mahawala, S. Vakkalanka, S. Jeedigunta, C. S. Ferekides, D. L. Morel; Thin Solid Films **480-481**, 466 (2005).
[6] J. E. Lewis, I. E. Ture, A. W. Brinkman, J. Woods; Semicond. Sci.Technol. **1,** 213 (1986).
[7] D. P. Padiyan, A. Marikani, K. R. Murali; Mater. Chem. Phys. **78,** 51(2002).
[8] K. R. Murali, K. Srinivasan, D. C. Trivedi; Mater. Sci. and Eng., **B11** 1 (2004)**.**
[9] K. R. Murali, K. Srinivasan, D. C. Trivedi; Mater. Letters **59,** 15 (2005).
[10] T. Elango, V. Subramanian, K. R. Murali; Surface and Coatings Technology **123,** 8 (2000).
[11] C. D. Lokhande, Eun-Ho Lee, Kwang-Deog Jung, Oh-Shim Joo; Mater. Chem and Phys. **91,** 200 (2005).
[12] O. Catzadilla, M. Zapata-Torres, L. Narvaez, S. Jimrnez, F. Rabago; Superficies y Vacio **14**, 35 (2002).
[13] R.W. Glew, Thin solid films, **46** 59 (1977).
[14] S. Tolansky; Multiple beam Interferomerty of surfaces and films, (Oxford Uni. Press, London, 1948).
[15] M. N. Borah, S Chaliha, P. C Sarmah, A Rahman, Indian J Pure & Appl Phys. **45**, 687 (2007).
[16] W. R. Runyem, Semiconductor measurements and Instrumentation, (Mc Graw Hill Book Company, New York, 1975) p. 144.
[17] P. C. Sarmah, A.Rahman, Bull. Mater. Sci., **21** 149 (1998).
[18] R. K. Swank, Phys. Rev. **153**, 844 (1967).
[19] S. M. Sze, Physics of Semiconductor Devices, 2nd Ed. (Wiley Eastern limited, New Delhi), pp. 126 (1983).
[20] E. H. Rhoderik, Metal semiconductor contacts (Clarendon Press, Oxford) p. 7 (1978).
[21] J. M. Pawlikoski, Thin Solid Films **190**, 39 (1990).
[22] J. Bardeen, Phys. Rev., **71,** 717 (1947).
[23] G. Wary, T. Kachary, A. Rahman, International Journal of Thermophysics, **27**, 332 (2006).
[24] Ting L. Chu, Shirley S. Chu, Sol Stat. Electron. **38**, 533 (1995).
[25] J. Dutta, D. Bhattacharyya, S. Chaudhuri, A. K. Pal, Sol. Energy Mat. And Solar Cells, **36**, 357(1995).

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